Business from technology

Printable, organic, and large-area realisation of integrated circuits

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PLASTIC ELECTRONICS CONFERENCE
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Outline

- VTT in brief
- Bench marks for high-volume OFET production
- VTT's focus in OFET fabrication development
- EU funded approach for printed, organic, and large area realisation of integrated circuits – aims and targets
- OFET fabrication by NIL
- Manufacturing platform development for organic electronics
- Circuit design and development

VTT Technical Research Centre of Finland in brief

Personnel 2920 ■ Turnover 276 M€ (budget for 2010)

Customer sectors

- Biotechnology, pharmaceutical and food industries
- **Electronics**
- Energy
- ICT
- Real estate and construction
- Machines and vehicles
- Services and logistics
- Forest industry
- Process industry and environment

Focus areas of research

- Applied materials
- Bio- and chemical processes
- Energy
- Information and communication technologies
- Industrial systems management
- **Microtechnologies and electronics**
- Technology in the community
- Business research

VTT's operations

Research and Development ■ Strategic Research ■ Business Solutions ■ IP Business ■ Corporate Services

VTT's companies

VTT Expert Services Ltd ■ VTT Ventures Ltd ■ VTT International Ltd

Benchmarks on the road towards high volume production of OFETs

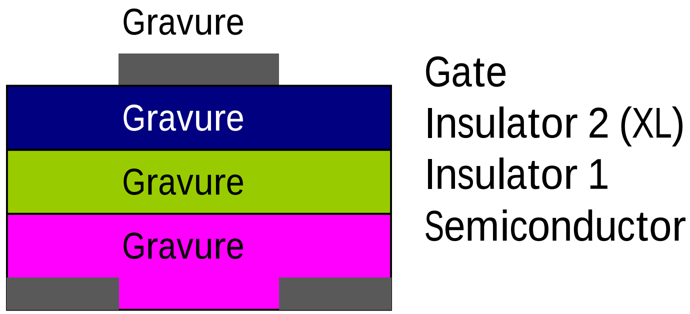
- Ring oscillator fabricated completely by means of mass-printing technologies
- 7-stage ring oscillator with frequency of 4 Hz
- Channel length 100 µm

layer	material	method
1 substrate	PET	-
2 source/drain	PEDOT:PSS	offset
3 semiconductor	F8T2	gravure
4 low-k dielectric	BuS*	gravure
5 high-k dielectric	Luxprint	flexo
6 gate	Ag-ink	flexo

A.C. Huebler et al. Org. Electronics 8, pp. 480-486, 2007

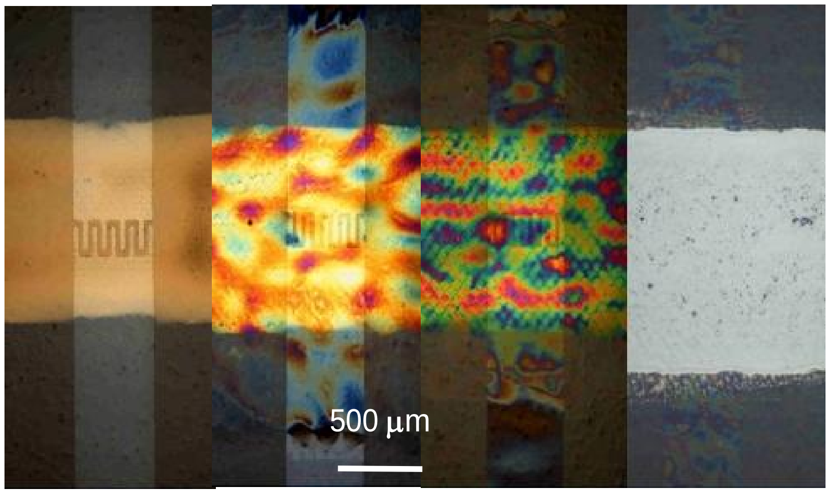
Benchmarks on the road towards high volume production of OFETs

- OFETs fabricated by the sequential gravure printing of polythiophene, two insulator layers, and a metal ink gate



- Bottom electrodes photolithographically patterned ITO drain and source contacts

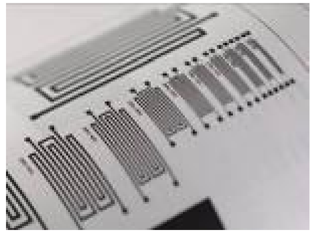
- Channel length 30 – 50 µm



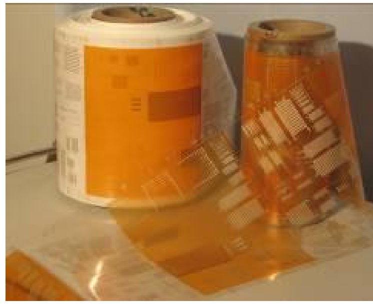
M. Voigt et al, Adv. Funct. Mat., 20 (2), 239-246, 2010

Conclusions based on the state-of-the-art in high-volume compatible OFET fabrication

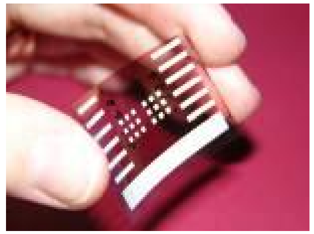
- Material improvement still needed, especially in upscaling and formulation for large-scale manufacturing



- Downscale the feature sizes of organic electronic components and circuits



- Develop OFET technology towards reliable and repeatable large-scale manufacturing without compromising performance
- Develop large-scale manufacturing consepts for organic complementary technology



- Development of design, testing, and standardisation of organic electronics

Roll-to-Roll Pilot facilities at VTT

PICO 2003

- 2 gravure printing units
- R2R hot embossing unit
- Corona and lamination units
- Drying units (air, UV, IR)
- Web width 200 mm
- Max. web velocity 100 m/min
- Installed in clean room (ISO7)

ROKO 2007

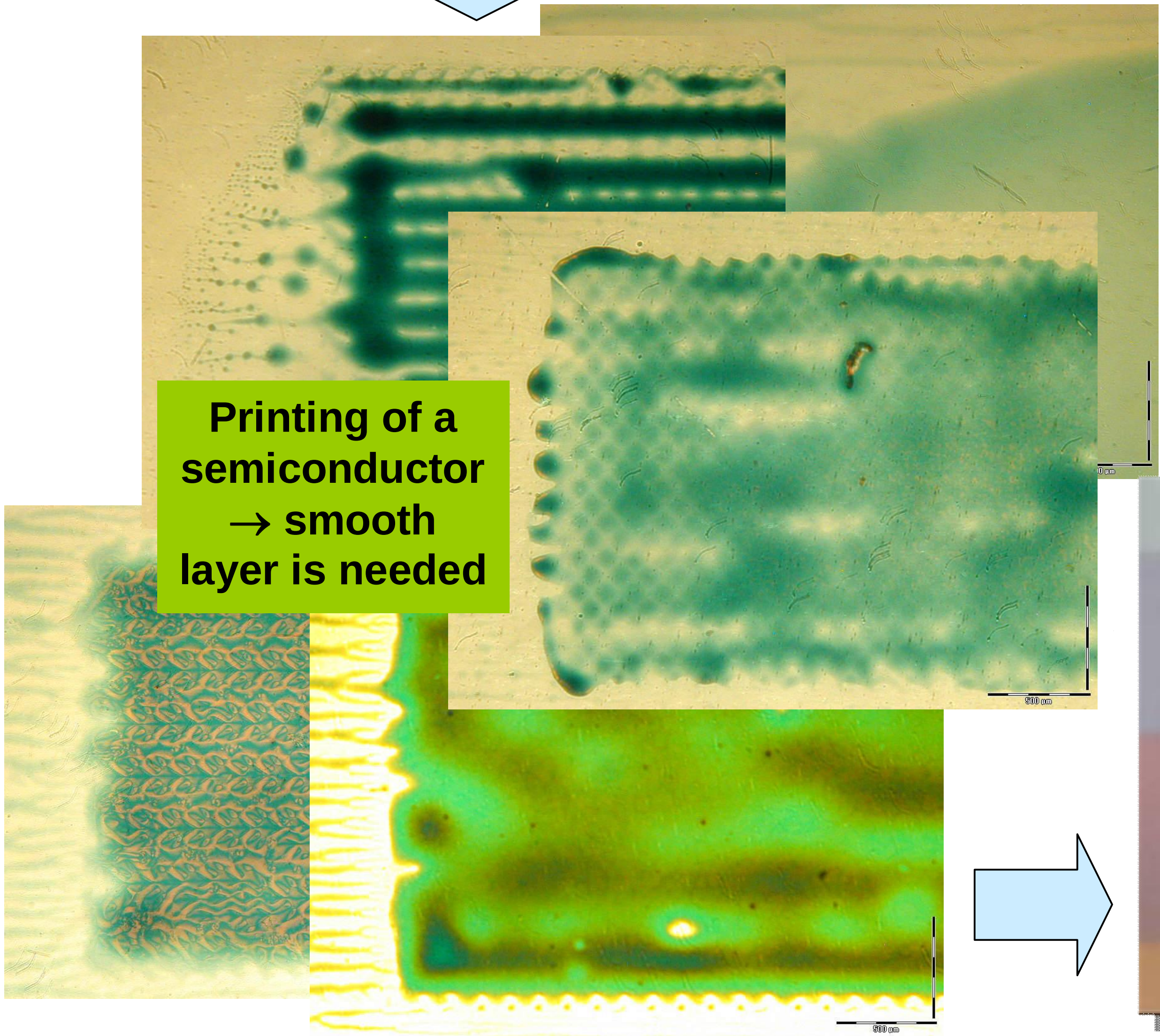
- 4 replaceable printing units
  - **Gravure, rotary screen, and flexography units**
- Corona and lamination units
- Drying units (air, UV, IR)
- Web width 300 mm
- Max. web velocity 10 m/min

+ 2012 Pilot hybrid production facility
- **R2R compatible die/flip-chip bonding**
- **Injection moulding**

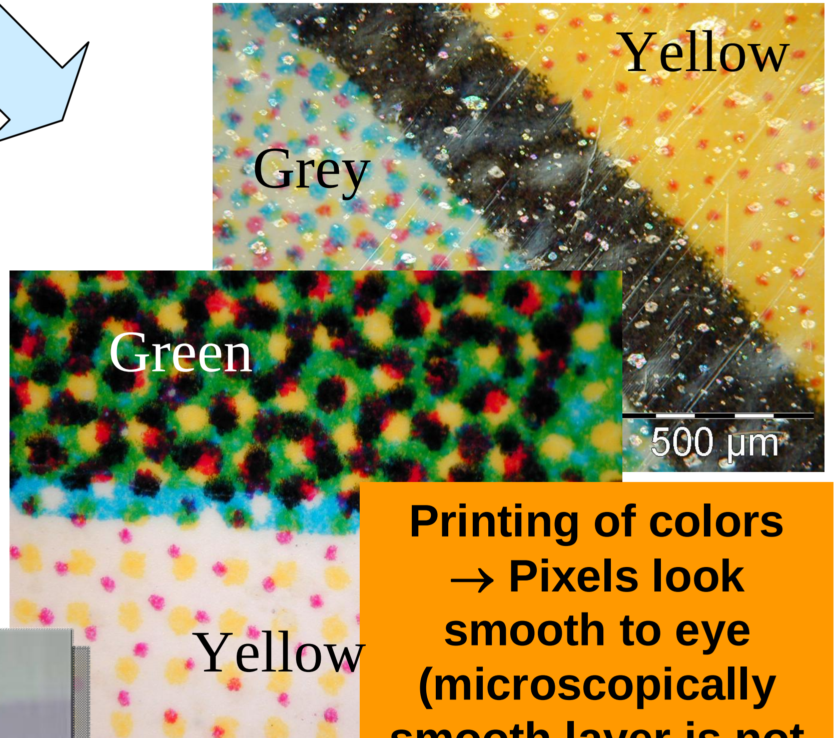
Pilot Production Facility 2010-

- Pilot production machine
  - **4 replaceable printing units, rotary cut, hot embossing, lamination units**
  - **Web velocity 0.1…30 m/min**
- Three unit inert gas atmosphere printing machine
  - **Gravure and rotary screen units**
  - **Oxygen level below 1000 ppm**
- R2R evaporation system
  - **5 thermal evaporation sources**

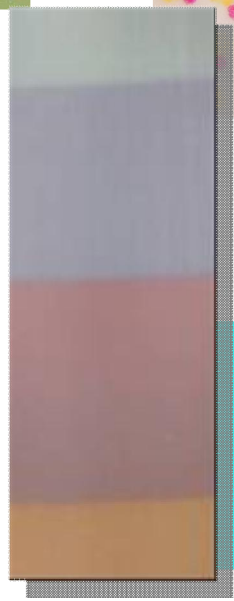
Printing of electronics vs. traditional printing



Printing of a semiconductor → smooth layer is needed



Printing of colors → Pixels look smooth to eye (microscopically smooth layer is not needed)



Smooth layers by ink and process development

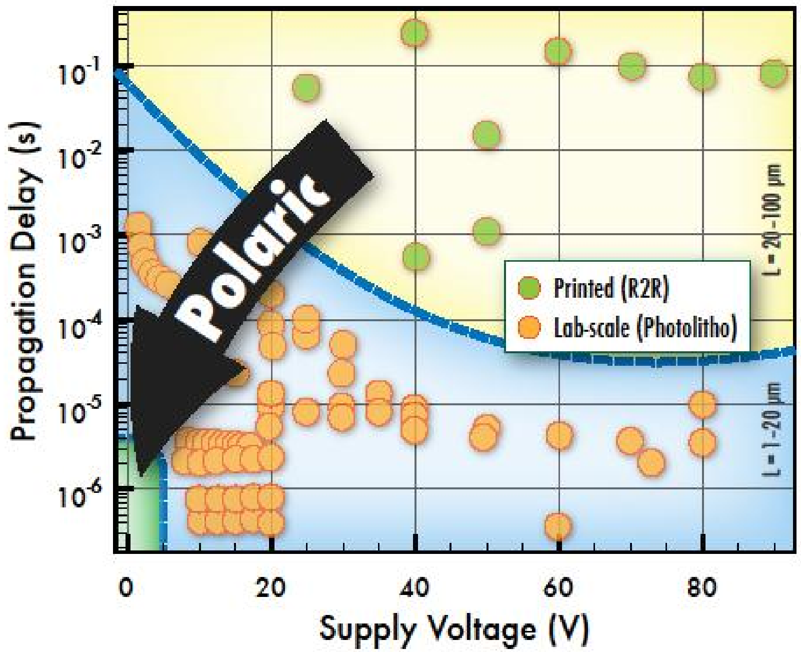
POLARIC – EU FP7
Printable, organic and large-area realisation of integrated circuits

POLARIC aims for increasing the **performance** of organic electronics and take steps towards high volume fabrication.

DEMONSTRATION BY LARGE-AREA PROCESSING METHODS ON FLEXIBLE SUBSTRATE	
Target specification	**POLARIC target**
Insulator layer thickness	**< 100 nm**
Transistor channel length	**< 1 µm**
Operation voltage for an organic IC	**< 5 V**
Organic complementary inverter circuits printed continuously and reliably	**Demonstrated**

→ Demonstrators: active matrix LCD & RFID tag

The POLARIC target compared to the current state-of-the-art in organic electronics.



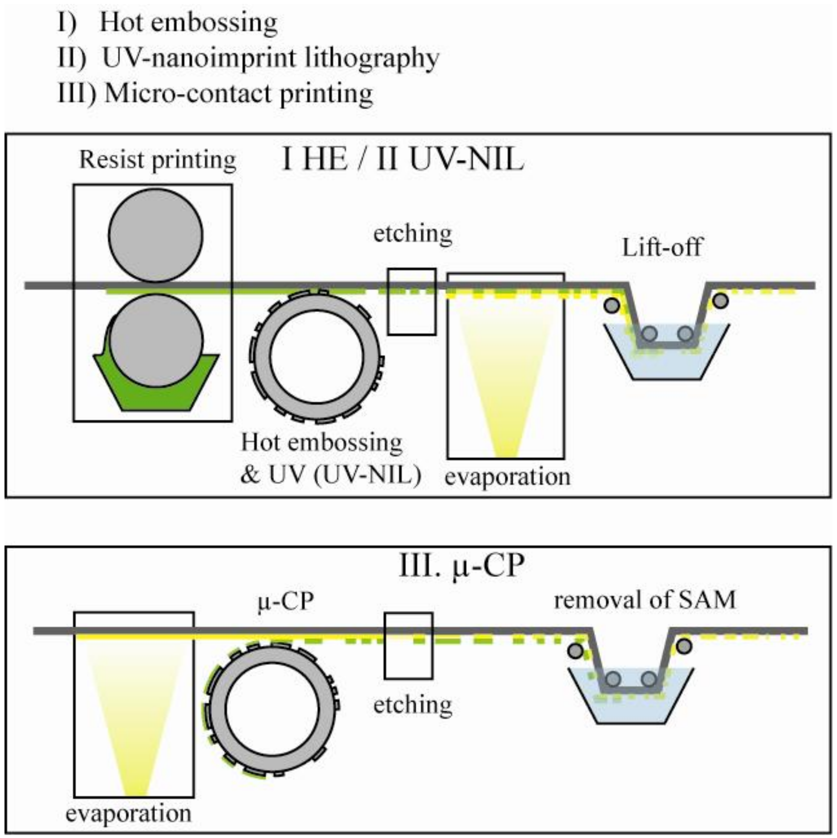
Nanoimprint lithography – the method for submicrometer patterning in R2R

Hot embossing and UV-NIL

1. Shim with nanoscale features is pressed against resist and shim cavities are filled
2. Permanent deformation by heat (in hot embossing) or light (in UV-NIL)
3. Etching of resist residuum might be needed to complete pattern transfer

Microcontact printing

- Additive printing of self-assembly monolayer
- Careful control of adhesion needed



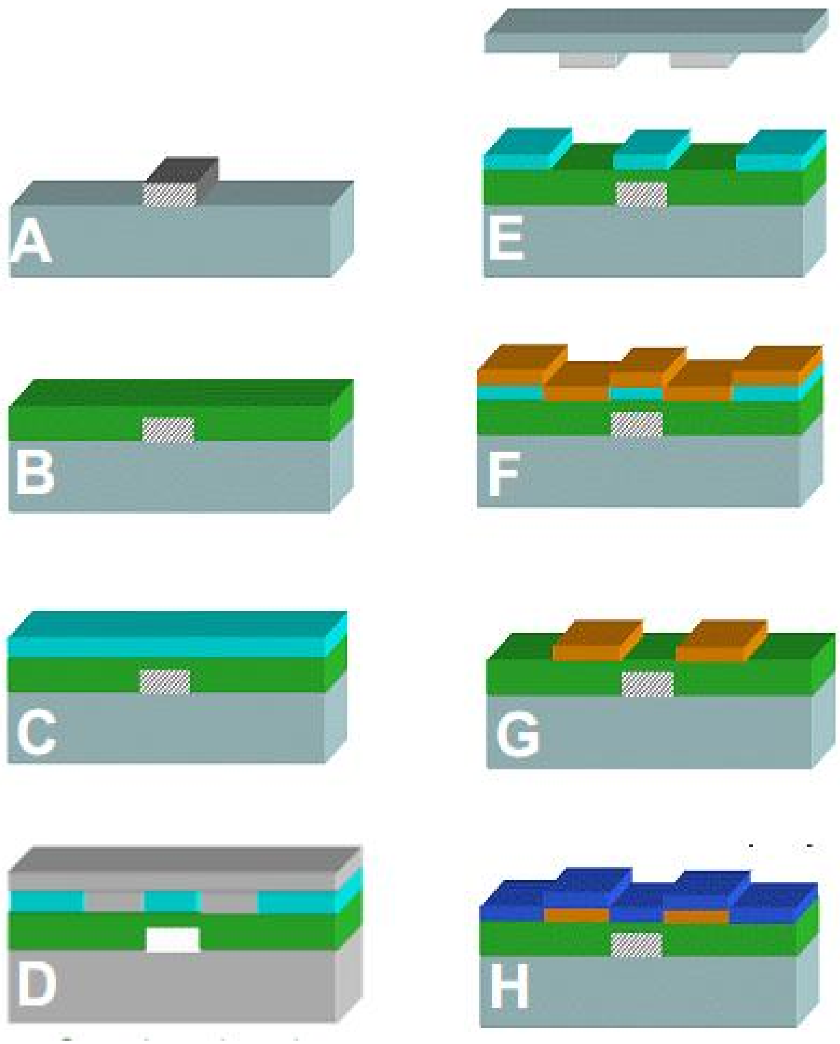
OFET fabrication by NIL

A gate structuring

B dielectric deposition

C resist deposition

D hot-embossing or UV-NIL



E stamp release

F metal evaporation

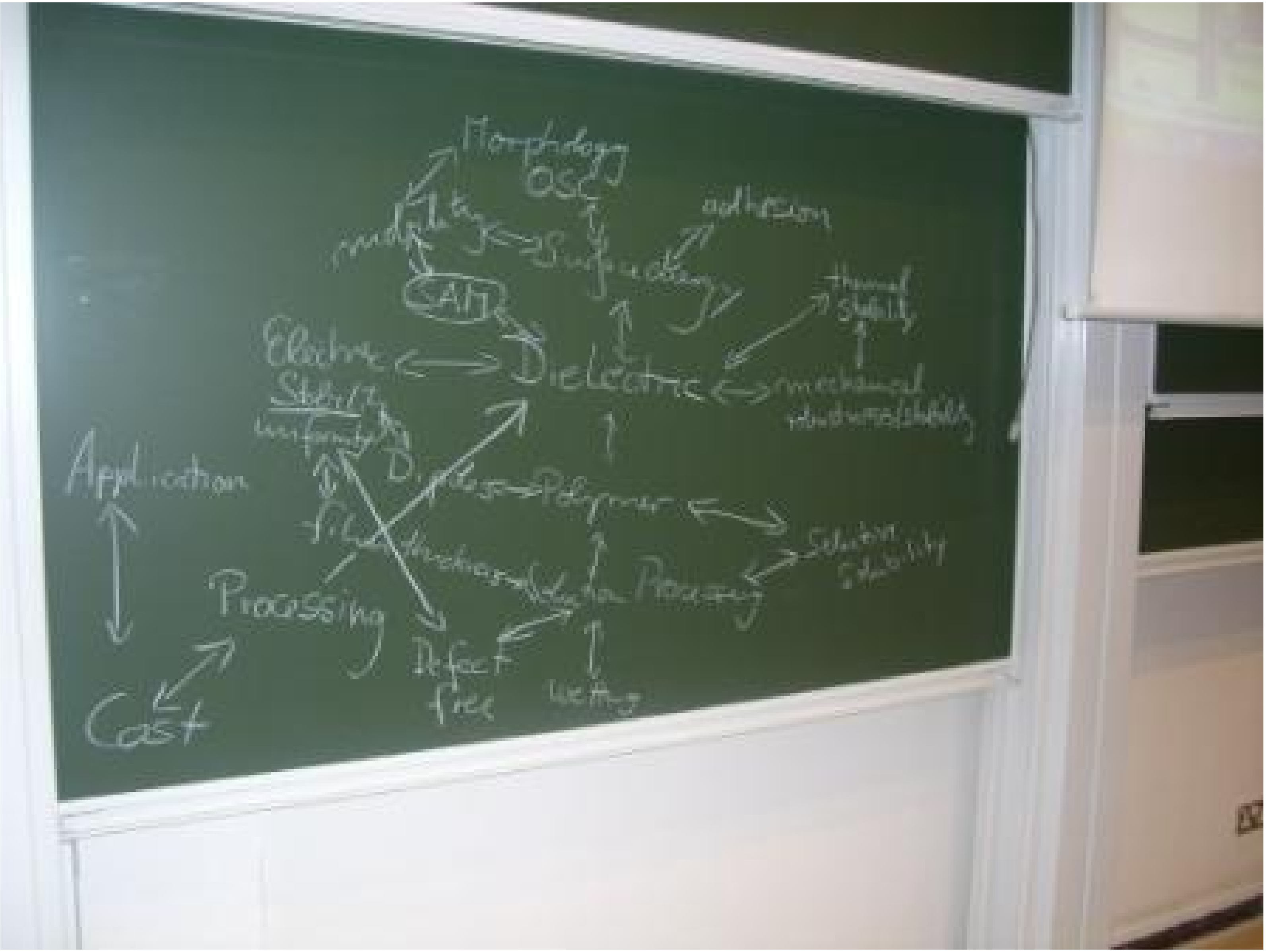
G lift-off

H semiconductor deposition

C. Auner et al., Org. Electronics 11, 552 (2010), by Joanneum Research Forschungsgesellschaft mbh

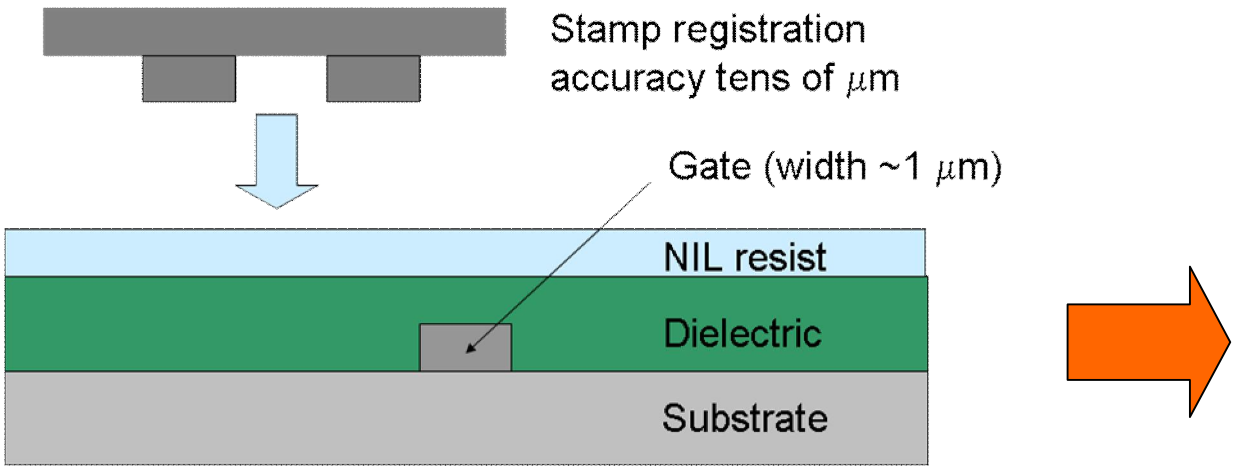
Dielectric deposition – things to consider

Goal: < 100 nm



OFET fabrication by NIL in roll-to-roll

- Channel lengths can be scaled down, but not the registration accuracy in R2R equipment
- Self-aligned R2R transistor process needed



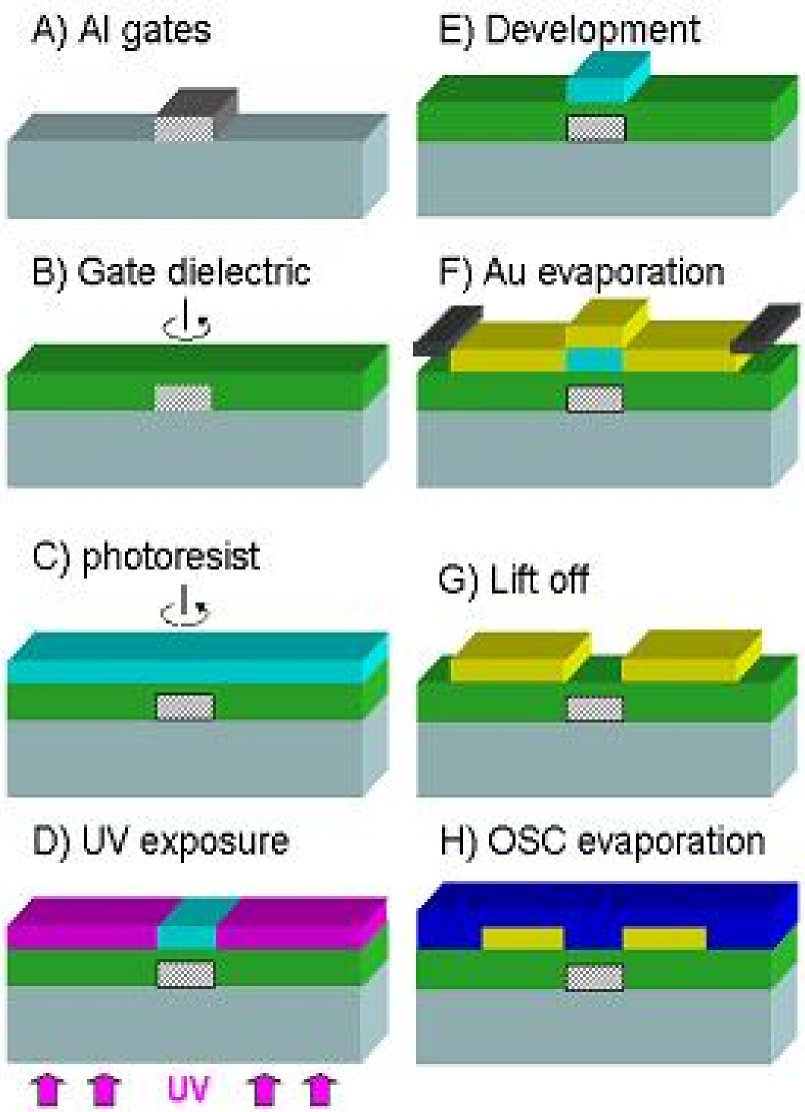
Component failure

Benefits of self-aligned R2R fabrication concepts for OFETs

- OFET cut-off frequency proportional to 1/L and $1/C_p$, where L is channel length and C_p parasitic capacitance
- Parasitic capacitance can be decreased by minimising the overlap between gate and source/drain electrodes
- Patterning of the gate and registration of the electrodes needed
- However, registration accuracy improvement in R2R equipments limited

→ Need for self-aligned R2R OFET fabrication concept

Self-aligned OFET fabrication by NIL



A
1. printing of resist on top of substrate
2. nanoimprinting/embossing
3. etching of resist residuum
4. metal evaporation (Al, Au, Ag, Cu) of gate and wiring
5. lift-off

B
6. printing of insulator layer(s)
7. laser ablation for vias

C
8. printing of resist

D
9. UV-exposure of resist (self-aligning process → gate functions as a mask)

E
10. Devepolment of the resist

F
11. metal evaporation (Al, Au, Ag, Cu) of source, drain and wiring

G
12. lift-off

H
13. printing of semiconductor

U. Palfinger et al., Adv. Mat. 22, in press, by Joanneum Research Forschungesellschaft mbh

Considerations regarding self-aligned processing

- Complete circuitry adds complexity (in respect to the basic transistor fabrication)
- E.g. even simplest backplane layout require many more process steps and true multilayer processing
- Usually every layer needs patterning and registration $\rightarrow$ limitation to the resoluton of the application

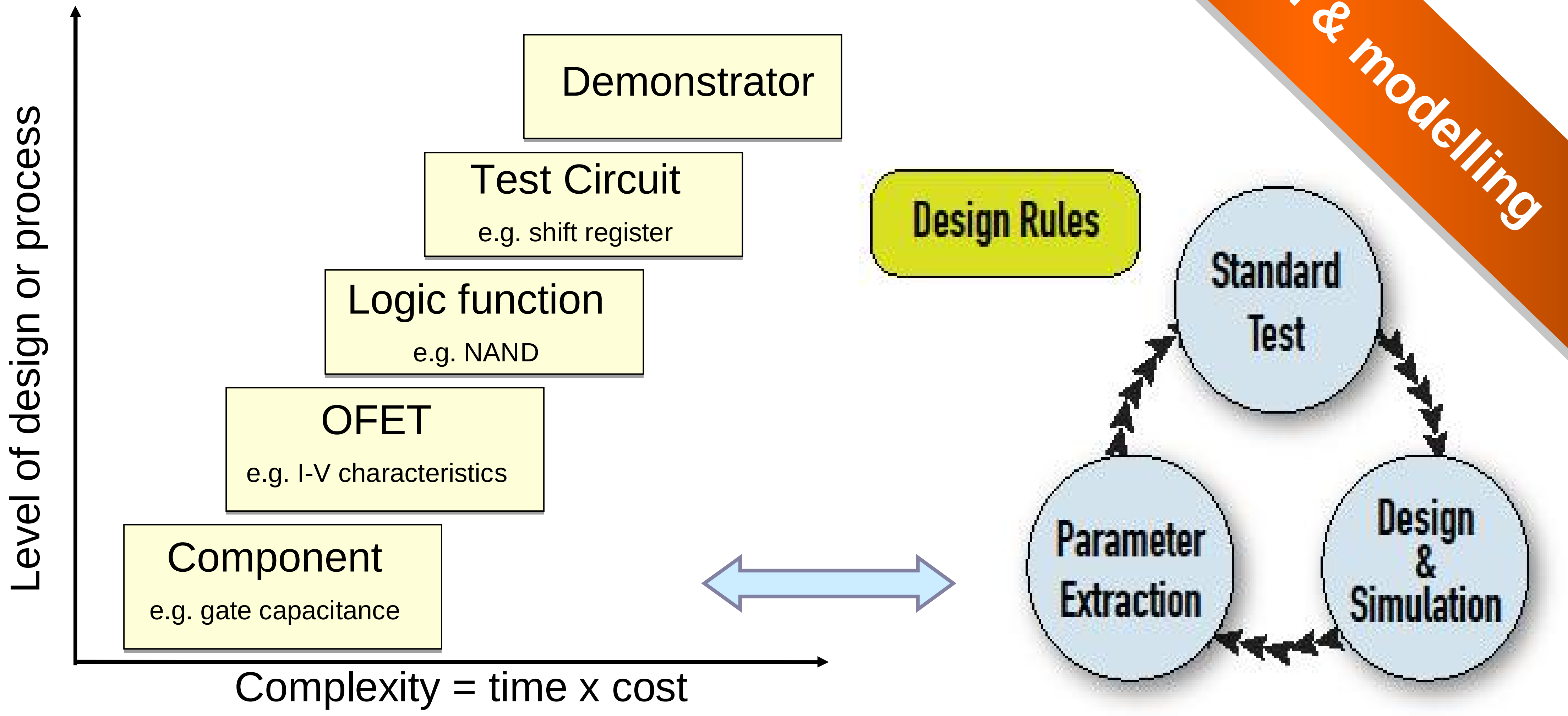
Development of manufacturing platforms for OFETs

Goal: R2R tooling

- Integration of nanoscale and millimeter scale dimensions
- Development of focused ion beam techniques to realise Ni shims for large-area roll-to-roll based NIL processing
- Transfer of laboratory scale key component processes and materials to large scale manufacturing
- Environmental evaluation and disposability

Circuit development

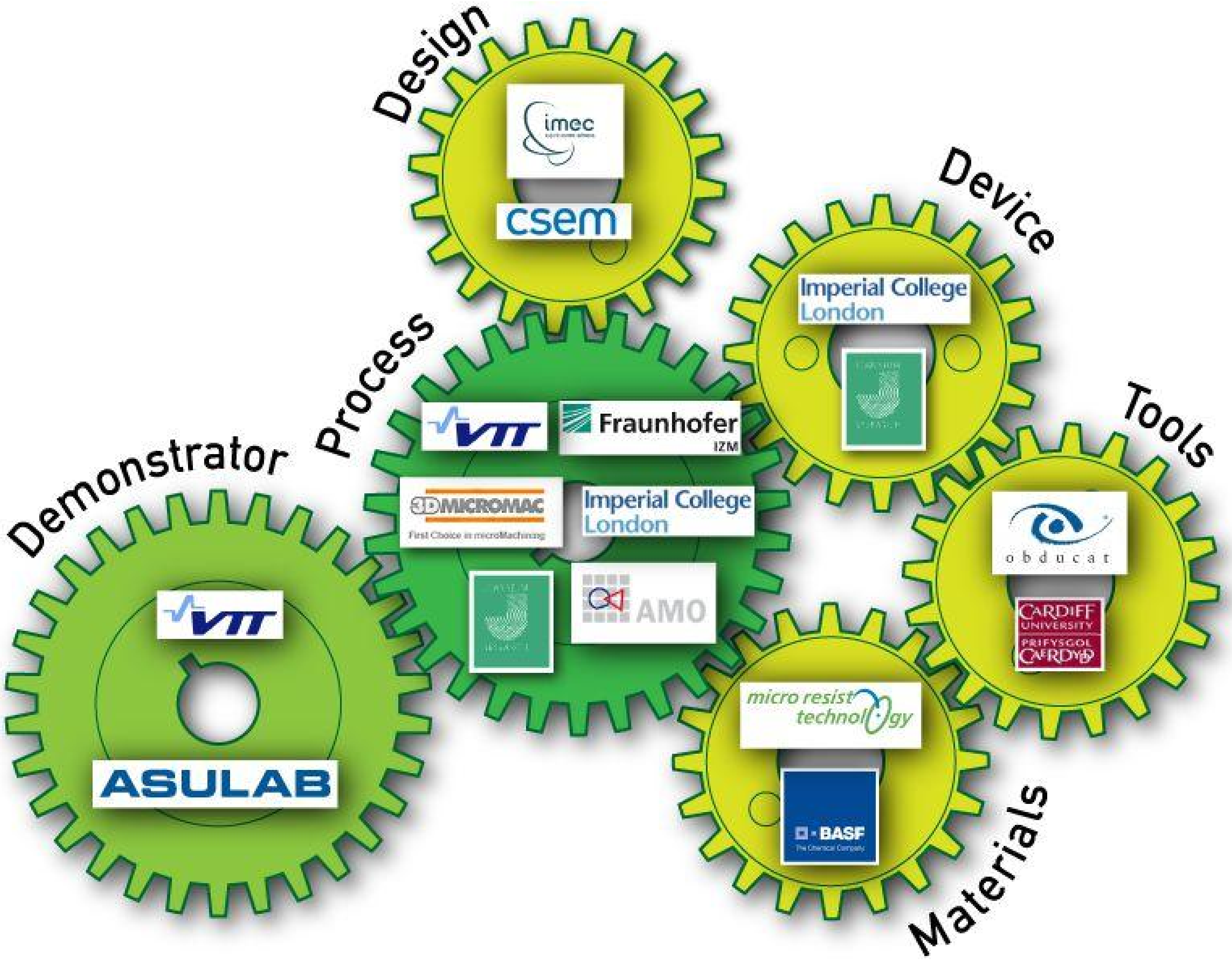
Goal: Design & modelling



Project partners

VTT Technical Research Centre of Finland (coordinator)
3D-Micromac
AMO
BASF
CSEM
Cardiff University
Fraunhofer-Gesellschaft IZM
IMEC
Imperial College London
Joanneum Research
micro resist technology
Obducat Technologies
Asulab, a division of The Swatch Group Research and Development Ltd.

Roles of the partners



Acknowledgements

- POLARIC EU project partners

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