System-level modelling and exploration

Managing application and platform complexity

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Business from technology

Outline

- **Motivation**
- **System-level modelling**
- **System-level exploration**
- **Example: GENESYS**
- **Example: ABSOLUT**
- **References**
- **Acronyms**

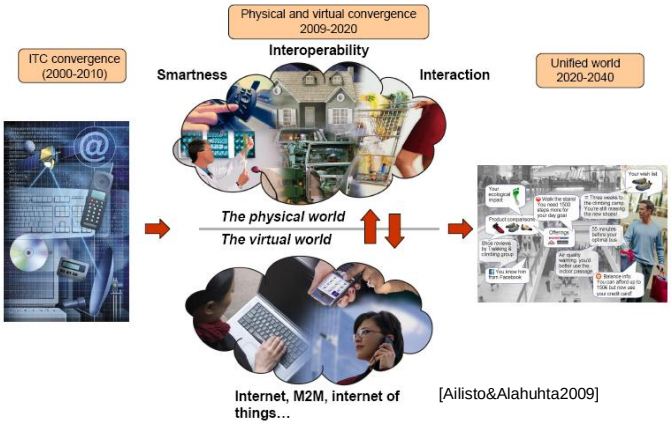
Application [1]

- Computing and communication technologies have enabled
  - Large amounts of data
  - Large amounts of users
  - Challenging applications
  - Increase of mobile use
  - Numerous applications per mobile device or accessed by it
  - Ubicomputing
- Further evolution requires improvements e.g. in
  - Parallel computing
  - Communication capacities
  - Networking
  - Power

Growth of application requirements exceeds that of technology capacity

Application [2]

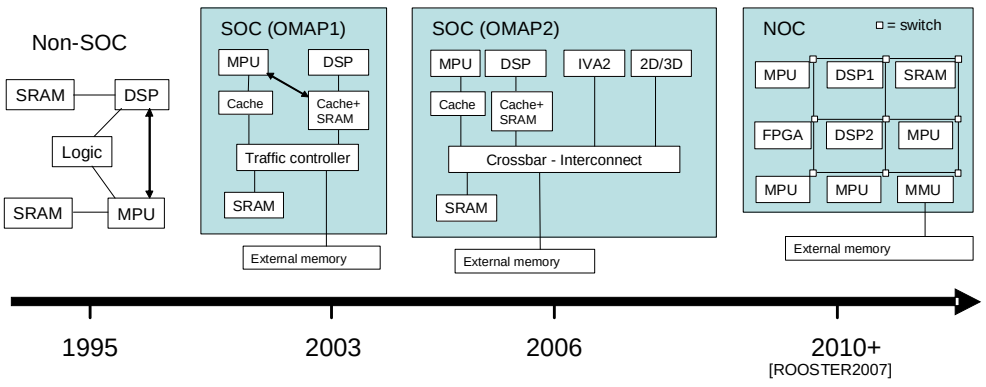
- **Ubicomp = ubicomputing + ubicommunication**



[Ailisto&Alahuhta2009]

…and Increasing

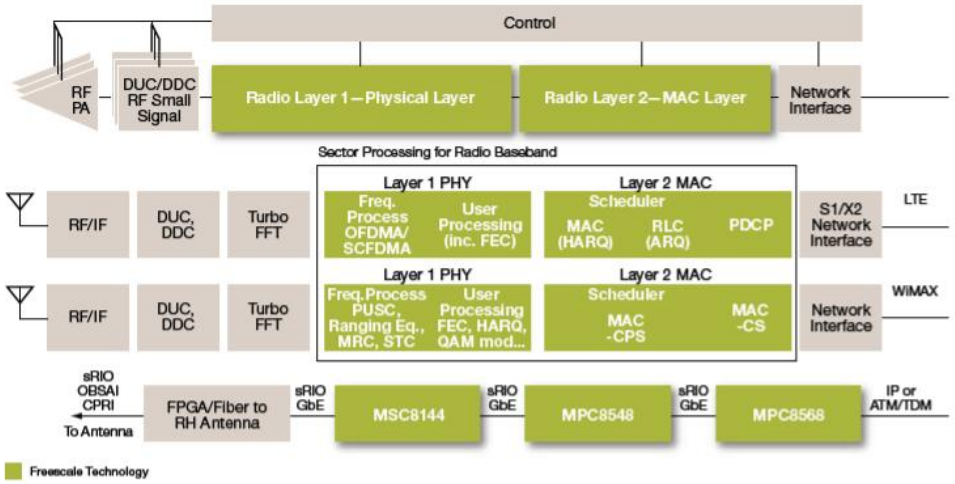
Architecture [1] – Smart phone application processor



[ROOSTER2007]

Architectures provide more capacity and become more complex

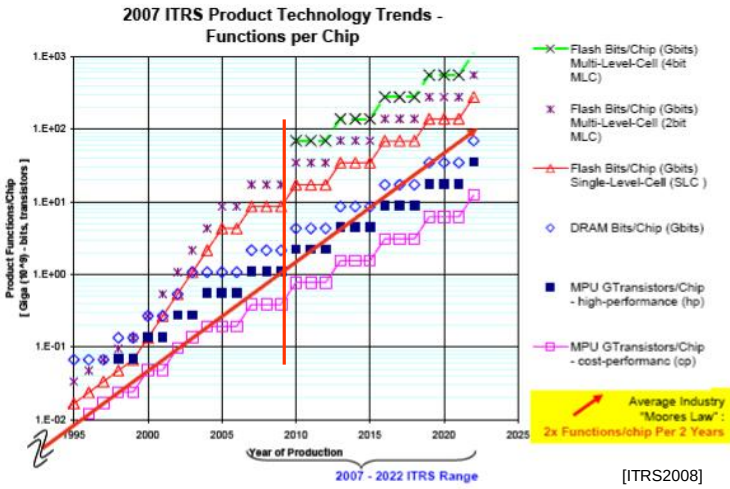
Architecture [2] – LTE/WIMAX base station



Even more capacity and more complex Source: www.freescale.com

Technology [1]

Product Function Size Trends



[ITRS2008]

Technology [2]

Consumer Portable Processing Performance Trends

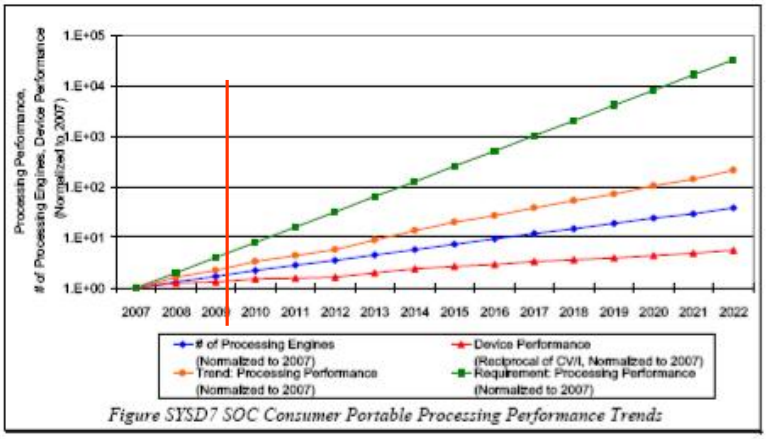


Figure SYSD7 SOC Consumer Portable Processing Performance Trends

[ITRS2008]

System-level modelling

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Embedded/electronic system-level modelling concepts

- **System-level modelling** uses models to conceptualize and construct systems
  - Separation of concerns, i.e. function vs. architecture, computation vs. communication
    - Application model
    - Platform model
    - Allocation/mapping model that links the two above to system-level model
- **System-level exploration** exercises system-level models to derive estimates of quality properties, e.g. functional correctness / efficiency, performance and power / energy
- **Electronic system level** (ESL) is a set of complementary methodologies that enable embedded system design, verification, and debugging
- **Transaction-level modelling** (TLM) is a high-level approach to modelling digital systems where details of communication among modules are separated from the details of the implementation of functional units or of the communication architecture

Source: www.wikipedia.org

Why system-level modelling ?

- **Quantitative and qualitative complexities** of current embedded systems and products are already huge and rising, e.g.
  - More and more **functionality** integrated in personal devices and networked devices becoming computing platforms
  - Dedicated chips contain hundreds of **processing engines** and general purpose multi-/many-core chips soon to exceed hundred processing engines
- Complexity issues can be **alleviated by modelling**:
  - **Abstraction** - simplification by focusing only on those properties that are relevant for the given purpose
  - **Partitioning** - division of a problem into nearly independent parts that can be studied in isolation
  - **Segmentation** - temporal decomposition of behaviour into smaller parts that can be processed separately
- **Models** are abstractions and created for certain purposes in order to limit the scope and keep models manageable

Examples of languages, methods, processes and tools

Languages
- UML
- SysML
- UML MARTE
- UML for SoC
- C
- C++
- SystemC
- SystemVerilog
- VHDL
- Matlab
- AADL
- Esterel
- And more

Methods
- ROOM
- OOSE
- TLM2
- MCSE
- Metropolis
- MDE
- MDA
- CSP
- And more

Processes
- Waterfall
- Spiral
- V
- RUP
- Y
- And more

Tools
- Mathworks
- # UML
- # SysML
- Telelogic
- Rational
- Papyrus
- Esterel Studio
- CoFluent Studio
- CoWare
- Virtutech Simics
- Mirabilis
- Carbon Design Systems
- OVP
- And more

System-level exploration

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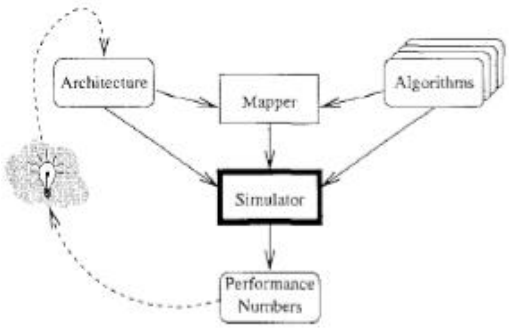
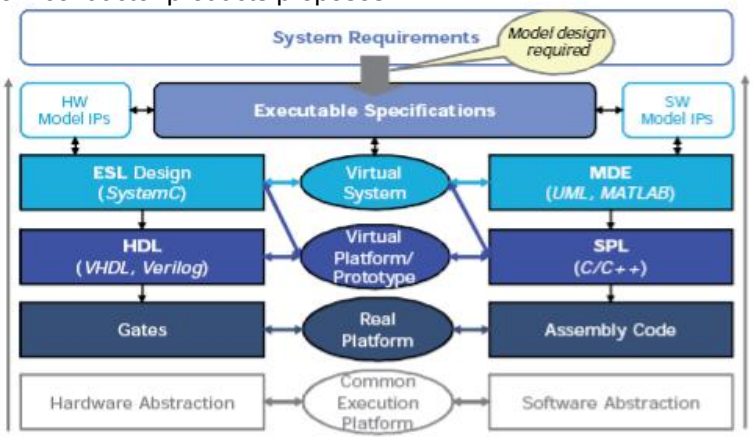
Y-chart approach

- Proposed in [Kienhuis1997] for quantitative analysis of application-specific dataflow architectures
- Applied since then widely in research work and also in commercial tools



CATRENE: Electronic System Level (ESL) flow

- The 2009 European Roadmap for design automation in semiconductor products proposes:



[CATRENE2009]

Example

GENESYS

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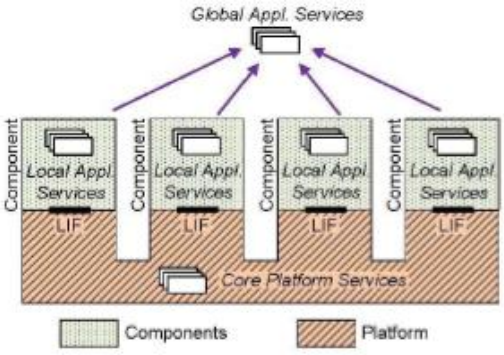
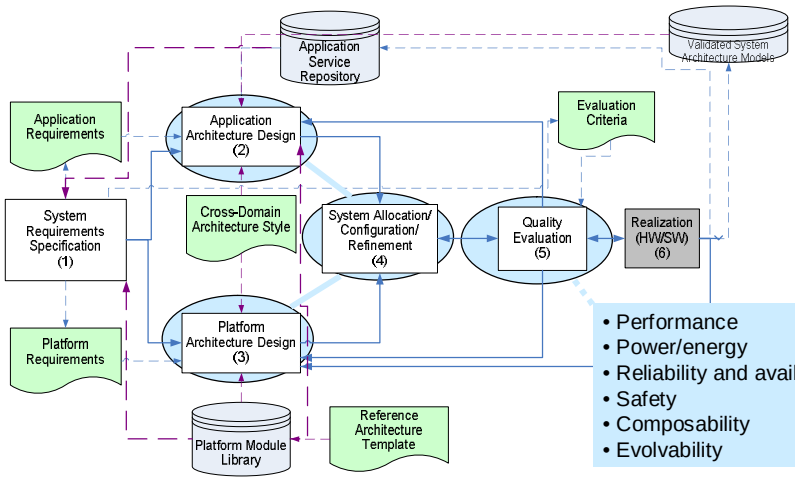
GENESYS – Generic embedded systems platform

- EU FP7 project GENESYS has defined architectural style and reference architecture template that supports component-based design style and composition of systems out of components
- GENESYS modelling approach follows architectural style and exploits services from libraries
  - Model- and quality-driven
  - Applies Y-chart
  - Uses UML MARTE profile for application, platform and allocation modelling
  - Uses SystemC in performance simulation



[GENESYS2009b]

GENESYS modelling approach



[GENESYS2009a]

Example

ABSOLUT

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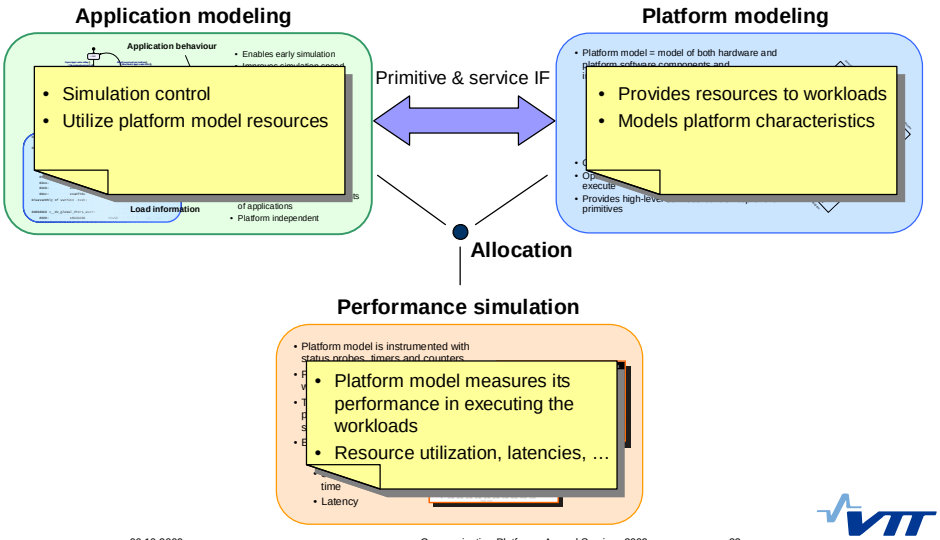
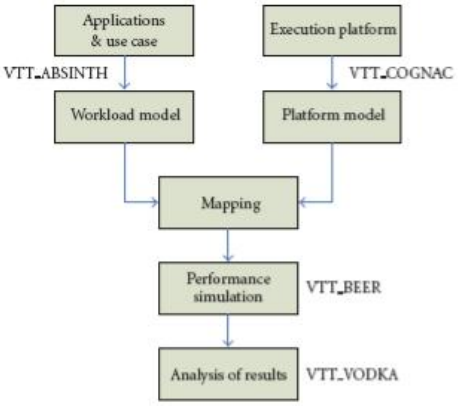
ABSOLUT: Application – platform performance modelling and evaluation

- A layered approach for workload-based performance simulation
  - Workload modeling
  - Platform modeling
  - Performance simulation at transaction level
- Aims at early evaluation, low effort, rapid simulation
  - Workload models can be created with little effort from e.g. source code
  - Tool support for creating complex platforms from model library
  - Does not require final SW or HW to exist
  - The amount of work required for simulating use cases is far less than comparable implementation efforts
- Validated with several case examples, where the difference between simulated and measured results has been about 15% on average

ABSOLUT: Modelling the system for performance evaluation



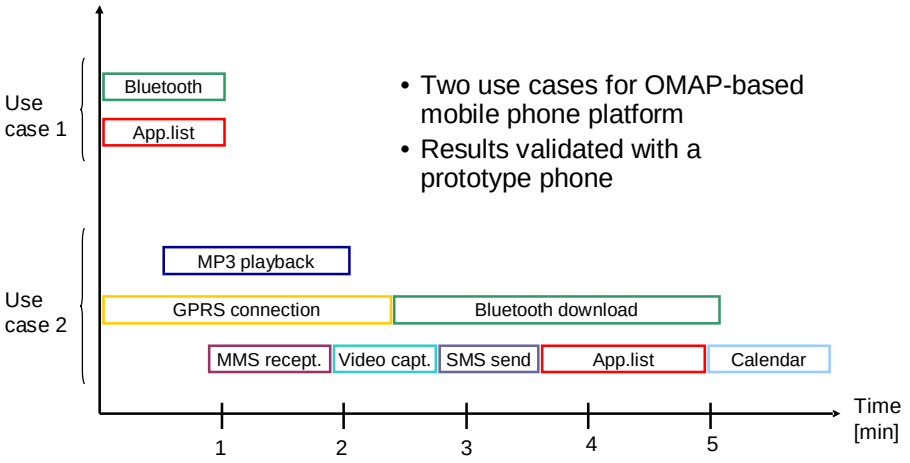
ABSOLUT: Tool support



- ABSINTH – Automatic workload generation
- COGNAC - platform model configuration from a library of performance models
- BEER - SystemC simulation library extended with configurable instrumentation
- VODKA - simulation results selection for analysis and viewing

[Kreku2008]

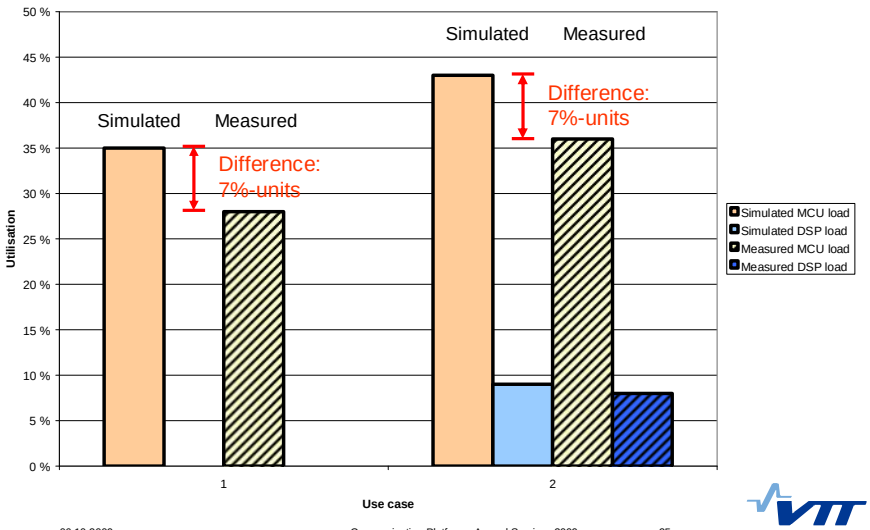
ABSOLUT: Mobile phone case example [1/2]



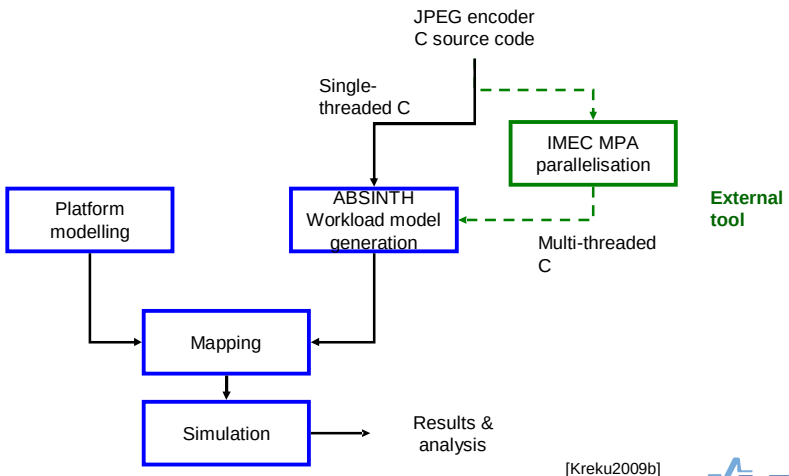
- Two use cases for OMAP-based mobile phone platform
- Results validated with a prototype phone

[Kreku2009a]

ABSOLUT: Mobile phone case example [2/2]

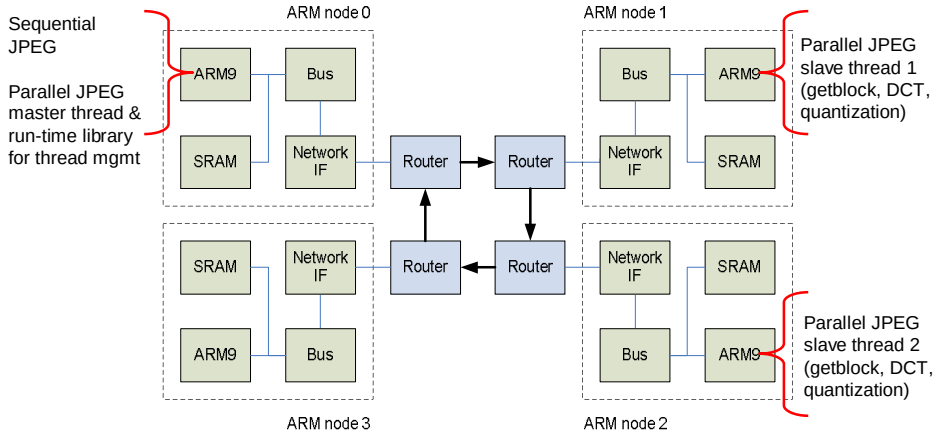


ABSOLUT: JPEG encoder case example [1/3]



[Kreku2009b]

ABSOLUT: JPEG encoder - Execution platform [2/3]



ABSOLUT: JPEG encoder – Parallelisation results [3/3]

Parallelisation		Seq.	Par-1	Par-2	Par-3
Execution time [ms]		69,5	55,3	38,7	53,9
Speedup wrt Seq.		1,00	1,26	1,80	1,29
IMEC MPA HLS speedup wrt Seq.		1,00	1,66	2,50	1,66
Node 0 utilisation	ARM	100 %	100 %	88 %	100 %
	SDRAM	59 %	55 %	43 %	53 %
	Bus	34 %	36 %	29 %	35 %
Node 1 utilisation	ARM	0 %	44 %	53 %	21 %
	SDRAM	0 %	23 %	31 %	11 %
	Bus	0 %	12 %	18 %	6 %
Node 2 utilisation	ARM	0 %	0 %	53 %	21 %
	SDRAM	0 %	0 %	31 %	11 %
	Bus	0 %	0 %	18 %	6 %

- Performance properties of whole system can be viewed
- Different application mappings and platfrom configurations can be explored

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Acronyms

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Some acronyms

- ABSOLUT - ABstract inStruction wOrkLoad & execUtion plaTform UML2/SystemC2-based performance simulation
- ABSINTH - ABStract INstruction exTraction Helper
- COGNAC - COnfiguration GeNerator for Absolut performanCe simulation
- BEER - Binary pErformance EvaluatoR
- VODKA - Viewer of collecteD Key information for Analysis

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Thank You !