Heterogeneous Technology Alliance

SOI MEMS Platform
Added value of HTA SOI MEMS Platform to customers

- Faster — because optimized use of existing process modules
- Lower cost — because utilizing existing equipment base
- Less risky — because wide base of expertise and solutions
- More innovative solutions — because access to wider technology portfolio
- AND effective industrialization and production capability
  One-stop shop
Attractive offering of HTA SOI MEMS Platform
One-stop shop

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Very extensive R&amp;D resources, 900 researchers</td>
</tr>
<tr>
<td>2</td>
<td>Can provide prototyping and process development</td>
</tr>
<tr>
<td>3</td>
<td><strong>Industrialization</strong> — bridging the gap between prototyping and production</td>
</tr>
<tr>
<td>4</td>
<td>Large set of process modules</td>
</tr>
<tr>
<td>5</td>
<td>Large set of <strong>SOI MEMS devices</strong> in offering</td>
</tr>
<tr>
<td>6</td>
<td>Large set of processing equipment with back-up/second source options</td>
</tr>
</tbody>
</table>
## SOI MEMS Platform

### VISION
- HTA offers leading SOI MEMS process platform for research, prototyping and pilot production as well as production ramp-up services

### MISSION
- Makes the large arsenal of tools available for customers and all HTA partners
- Bridging the gap between research and manufacturing
- Strengthening the European position in MEMS field
- Helping researcher to do their work, through networking, creating new projects, and fostering innovations.
Platform purpose and definition

- **Platform purpose**
  - To create flexibility in designing and manufacturing new components
  - Customer needs can be better met through joining our arsenal of capabilities
  - Open up our arsenal to all HTA partners

- **Definition**
  - Platform forms a basis for research and product development
  - Platform enables flexible processing capability and prototyping
Example of SOI MEMS fabrication cycle
Technical definition of SOI MEMS Platform

- This platform covers Silicon-on-Insulator (SOI) MEMS fabrication capabilities of all HTA partners
- Makes use of the properties of low stress single-crystalline silicon, where active structures are typically formed by deep reactive ion etching.
- SOI MEMS is typically used for
  - Silicon oscillators
  - Microphones, speakers
  - Compass, navigation, motion sensors
  - Sensors and actuators
  - Energy harvesting
  - Micro fuel cells, microfluidics
  - Other deep reactive-ion etched micro structures
**HTA SOI MEMS Platform**

**Market**
- Special needs
- Small scale products (SME)

**HTA facilities**

**External foundry**

**Customer needs**

**Resulting technology**

**Tech1**
- CSEM Neuchâtel (100 and 150 mm)

**Tech3**
- CEA LETI Grenoble (200 mm)

**Tech5**
- VTT Espoo (150 mm)

**Tech7**
- Fraunhofer (100, 150 and 200 mm)

**Product**

**R&D**

**TRL files**
M(O)EMS processing
Packaging

Wafer-level, 100~200 mm
Plastic
CMOS processing
Processing on specific substrates

- Organics
- Compound semicond.
- LTCC
### Applicable materials in MEMS fabrication facility

<table>
<thead>
<tr>
<th>Material</th>
<th>Chip-Level</th>
<th>100 mm Wafer-Level</th>
<th>150 mm Wafer-Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Glass</td>
<td>x</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>Ceramics (i.e. PZT, LTCC, ...)</td>
<td>x</td>
<td>x</td>
<td></td>
</tr>
<tr>
<td>Lithium Niobate / Lithium Tantalate</td>
<td>x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Others</td>
<td>x</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Saphire, SiC, Ge</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2&quot; wafer Saphire, SiC, Ge</td>
<td></td>
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</tbody>
</table>

### Front-End-of-Line

<table>
<thead>
<tr>
<th>Process Step</th>
<th>Chip-Level</th>
<th>100 mm Wafer-Level</th>
<th>150 mm Wafer-Level</th>
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</thead>
<tbody>
<tr>
<td>RCA clean 1 &amp; 2</td>
<td>x</td>
<td></td>
<td></td>
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<tr>
<td>Piranha clean</td>
<td>x</td>
<td></td>
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<tr>
<td>DI-H₂O flushing</td>
<td>x</td>
<td></td>
<td></td>
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<tr>
<td>Thermal Oxidation</td>
<td>x</td>
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<td></td>
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<tr>
<td>Dry</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Wet</td>
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<td></td>
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<tr>
<td>RTA</td>
<td></td>
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<tr>
<td>Chemical Vapour Deposition - CVD</td>
<td></td>
<td></td>
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<tr>
<td>SiO₂ - low pressure</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>SiO₂ - plasma enhanced</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Si₃N₄</td>
<td></td>
<td></td>
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<tr>
<td>Si₃N₄ - plasma enhanced</td>
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<tr>
<td>poly-Si</td>
<td></td>
<td></td>
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<tr>
<td>SION - plasma enhanced</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TEOS - plasma enhanced</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>alpha-Si - plasma enhanced</td>
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<tr>
<td>Arias</td>
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<tr>
<td>CentroTherm</td>
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<td></td>
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<tr>
<td>Heatpulse 610</td>
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<tr>
<td>LPT</td>
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<td>P5000 / Oxford</td>
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<td>P5000 / Oxford / Oxford</td>
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</tbody>
</table>

### Availability for different substrates and names of equipment

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Chip-Level</th>
<th>100 mm Wafer-Level</th>
<th>150 mm Wafer-Level</th>
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<tbody>
<tr>
<td>Saphire, SiC, Ge</td>
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<tr>
<td>2&quot; wafer Saphire, SiC, Ge</td>
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</tbody>
</table>

Example page of process step and equipment list to facilitate quick and efficient response.
CSEM contribution to SOI MEMS Platform

**Competitive edge**

- MEMS developments from R&D to industrialization since 1985
- ISO-certified fabrication procedures
- Activity ranging from R&D to small series production
- Highly flexible processing options
- System engineering through wide application portfolio
- Dedicated staff for MEMS project management, R&D and production
- First class reliability (HRXRD and microscopy) laboratory
- World-class partners through HTA and EU projects

**Technical description**

- Full processing capability for SOI-MEMS
  - SOI or cavity-SOI
  - 100 and 150 mm wafer size
  - Wide range of wafer bonding processes
  - Through-glass vias
  - i-line lithography (1 µm)
  - High-aspect ratio structures by DRIE
- Output: device wafers or diced device wafers
  - Internal and external options for packaging
- Future development
  - In-house wafer-level encapsulation
  - TSV
CSEM MEMS Device examples

- Precision micromechanical parts
- Production for several watchmakers

- Micromirror
- Commercialized by Sercalo

- Resonators from 32 kHz to 5 MHz

- Tunable blazed diffraction grating
- Blazing, tilted, mirror surfaces

\[ y = 0.000305x^3 - 0.023882x^2 + 0.004834x - 0.121196 \]

\[ R^2 = 0.999114 \]

- 70 kHz, passive compensation

\[ \delta = 0.005 \text{ ppm/}^\circ \text{C} \]

\[ \beta = -23.8 \text{ ppb/}^\circ \text{C}^2 \]

\[ \gamma = 305 \text{ ppt/}^\circ \text{C}^3 \]
CEA Leti contribution to SOI MEMS Platform

Competitive edge

- SOI Manufacturing knowhow since 1990
- Industrial type processing facilities
- Characterization and reliability platform
- Wafer level packaging and 3D integration line
- Experienced, well-trained personnel
- A strong experience in industrial transfers
- ISO 9001 certified
- World-class partners through HTA and EU projects

Technical description

- General process flow containing well-established sequences and steps
  - 200 mm wafer size
  - Thin and thick SOI wafer bonding cavity-SOI
  - Multi wafers assembly
  - Double side wafer stepper lithography (0.4 µm)
  - High-aspect ratio structures by DRIE
- Output: device wafers or diced device wafers
  - Wafer level hermetic packaging
  - Thin film packaging
  - TSV
- Future development:
  - 3D integration with electronics
Leti MEMS device examples

Inertial sensors

Gaz sensors array

3D force sensor

Resonators
VTT contribution to SOI MEMS Platform

<table>
<thead>
<tr>
<th>Competitive edge</th>
<th>Technical description</th>
</tr>
</thead>
<tbody>
<tr>
<td>• MEMS R&amp;D processing since 1991 and production for customers since 1997</td>
<td>• General process flow containing well-established sequences and steps</td>
</tr>
<tr>
<td>• ISO9001-certified fabrication procedures</td>
<td>• SOI or cavity-SOI</td>
</tr>
<tr>
<td>• Infrastructure meeting the standards of R&amp;D and small-medium scale production</td>
<td>• 150 mm wafer size</td>
</tr>
<tr>
<td>• Flexible practices for R&amp;D purposes</td>
<td>• i-line lithography (0.5 µm)</td>
</tr>
<tr>
<td>• Dedicated staff for research, wafer processing and maintenance</td>
<td>• High-aspect ratio structures by DRIE</td>
</tr>
<tr>
<td>• Strategic partnerships with key MEMS companies</td>
<td>• Plug-up –method and HF-vapor etching</td>
</tr>
<tr>
<td>• World-class partners through HTA and EU projects</td>
<td>• Design rules and standard processes (negotiable)</td>
</tr>
<tr>
<td></td>
<td>• Output: device wafers or diced device wafers</td>
</tr>
<tr>
<td></td>
<td>• Encapsulation with HTA partners</td>
</tr>
<tr>
<td></td>
<td>• Option: 3rd party encapsulation (e.g. VTI Technologies)</td>
</tr>
<tr>
<td></td>
<td>• Future development:</td>
</tr>
<tr>
<td></td>
<td>• In-house wafer-level encapsulation</td>
</tr>
<tr>
<td></td>
<td>• TSV</td>
</tr>
<tr>
<td></td>
<td>• 200 mm wafer size</td>
</tr>
</tbody>
</table>
VTT MEMS Device examples

- Magnetometer based on the Lorentz force
- Pressure sensor
  - CMOS monolithically integrated
- Resonator
  - Low phase noise, Q~120 000
- Carbon dioxide meter
  - Commercialized with Vaisala Oyj

FPI  Thermopile

VTT MEMS Device examples
FhG contribution to SOI MEMS Platform

Competitive edge

- More than 25 years experience in MEMS R&D
- Broad equipment base with flexible processes
- Experienced, well-trained personnel
- Customer specific processes can be developed and integrated
- Technology transfer to other fabs on customers demand
- Small scale production and medium-large scale production support
- 3 Shift operating for fast development
- ISO 9001:2008 certified, ISO/TS 16949 conformal (depending on the institute)
- Strategic partnerships with key MEMS companies
- World-class partners through HTA and EU projects

Technical description

- Technological experience for monolithically integrated MEMS and CMOS
- Clean Room for R&D and fabrication
  - Wafer size: 100, 150 and 200 mm
  - Wafer stepper lithography, mask aligner, High-aspect ratio structures by DRIE processes
  - Standard SOI and epi-poly-SOI
  - SOI wafer bonding and patterning, cavity-SOI (bonding and deep RIE)
  - Gas phase etching (HF or XeF2)
  - Wafer grinding and dicing (with IR-capability)
  - In house wafer level packaging (glass-frit, eutectic, direct, anodic bonding, metal thermocompression)
  - Vacuum package (also with getter material)
  - Wafer level test
- High temperature 1.0µm CMOS process based on thin film SOI for 250°C
- Smart Power (600V) process based on thin film SOI
- Single crystalline diodes based on SOI for microbolometers
- Future development:
  - Integration with electronics
  - Thin film encapsulation
Vacuum packaged 2D MEMS scanning mirror
(FhG ISIT Itzehoe)

Diode Bolometer
(FhG IMS Duisburg)
**Operation of the Platform**

- **Request by customer**
- **Local site**
  - P.M.1
- **HTA 2**
  - P.M.2
- **HTA 3**
  - P.M.3

**Key principles of operation**

- One-stop shop
- In case of multiple offers the partner who supplies the best offer from customer point of view will be used (delivery time, experience, cost, suitability of processing equipment)
- Information is also directly transferred between the specialists (platform managers are kept informed).

**Platform Manager’s (P.M.) role**

- Contact person and coordinator
- Acts as a matchmaker between the specialists
- Know-how of design rules
- Know-how of processing capabilities and limitations
- Pricing, scheduling, and resourcing
Access to Platform services

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